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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 42390.P8718 Total Pages 2

First Named Inventor or Application Identifier Byrd, et al.

Express Mail Label No. EL234218149US

ADDRESS TO: **Assistant Commissioner for Patents**
Box Patent Application
Washington, D. C. 20231

APPLICATION ELEMENTS
See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 17)
(preferred arrangement set forth below)
- Descriptive Title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 5)

4. X Oath or Declaration (Total Pages 5)

a. X Newly Executed (Original or Copy)

b. ___ Copy from a Prior Application (37 CFR 1.63(d))
(for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**

i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ___ Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ___ Microfiche Computer Program (Appendix)

7. __ Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. X Assignment Papers (cover sheet & documents(s))
9. __ a. 37 CFR 3.73(b) Statement (where there is an assignee)
__ b. Power of Attorney
10. __ English Translation Document (if applicable)
11. __ a. Information Disclosure Statement (IDS)/PTO-1449
__ b. Copies of IDS Citations
12. __ Preliminary Amendment
13. X Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. __ a. Small Entity Statement(s)
b. Statement filed in prior application, Status still proper and desired
15. __ Certified Copy of Priority Document(s) (if foreign priority is claimed)
16. __ Other: _____

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:
___ Continuation ____ Divisional ____ Continuation-in-part (CIP)
of prior application No: _

18. **Correspondence Address**
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FEE TRANSMITTAL FOR FY 2000

TOTAL AMOUNT OF PAYMENT ($) 916.00

Complete if Known:
Application No. ****
Filing Date 9/12/00
First Named Inventor Byrd, et al.
Group Art Unit ****
Examiner Name ****
Attorney Docket No. 42390.P8718

METHOD OF PAYMENT (check one)

1. [ ] **The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:**

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	690	201	345	Utility application filing fee	690.00
106	310	206	155	Design application filing fee	
107	480	207	240	Plant filing fee	
108	690	208	345	Reissue filing fee	
114	150	214	75	Provisional application filing fee	

SUBTOTAL (1) $ 690.00

2. EXTRA CLAIM FEES

		Extra Claims		Fee from below		Fee Paid
Total Claims	26	– 20** =	6	X 18.00	=	108.00
Independent Claims	4	– 3** =	1	X 78.00	=	78.00
Multiple Dependent					=	

****Or number previously paid, if greater; For Reissues, see below.**

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) $ 186.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Small Entity

Patent fees are subject to annual revisions. Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid.
See Forms PTO/SB/09-12

Fee Code	Fee ($)	Fee Code	Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for response within first month	
116	380	216	190	Extension for response within second month	
117	870	217	435	Extension for response within third month	
118	1,360	218	680	Extension for response within fourth month	
128	1,850	228	925	Extension for response within fifth month	
119	300	219	150	Notice of Appeal	
120	300	220	150	Filing a brief in support of an appeal	
121	260	221	130	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive unavoidably abandoned application	
141	1,210	241	605	Petition to revive unintentionally abandoned application	
142	1,210	242	605	Utility issue fee (or reissue)	
143	430	243	215	Design issue fee	
144	580	244	290	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Petitions related to provisional applications	
126	240	126	240	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40.00
146	690	246	345	For filing a submission after final rejection (see 37 CFR 1.129(a))	
149	690	249	345	For each additional invention to be examined (see 37 CFR 1.129(a))	
Other fee (specify)					
Other fee (specify)					

SUBTOTAL (3) $ 40.00

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SUBMITTED BY:

Typed or Printed Name: Charles K. Young

Signature Charles K. Young Date 9/12/00

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UNITED STATES PATENT APPLICATION

FOR

APPARATUS AND METHOD FOR PROGRAMMABLE LINE INTERFACE IMPEDANCE MATCHING

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APPARATUS AND METHOD FOR PROGRAMMABLE LINE INTERFACE IMPEDANCE MATCHING

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to the field of network circuitry. More particularly, the invention relates to a more versatile line interface for connecting a receiver to various transport mediums (e.g., data lines) hosting transport protocols that have different impedance requirements.

2. Description of Related Art

Various transport protocols are used to transport data across transport mediums. Transport protocols are defined by various industry specifications. For example, the T1 protocol (also called DS1) is specified by the American National Standards Institute (latest revision T1.403.00, 403.01, 403.02-1999). The E1 protocol (or E-1) is a European digital transmission format devised by the International Telecommunication Union (ITU-T) and is compliant with G703 (latest revision October, 1998). Similarly, the J1 protocol, used in Japan, is specified by the Telecommunication Technology Committee (latest revision JT-G703, April, 1989).

When a connection is made to a transport medium hosting a particular transport protocol, the line interface, or connector, must have a substantially similar impedance to that specified by the transport protocol, otherwise electrical reflection will occur causing interference, as is well known.

Figure 1 shows a prior art line interface for connecting a receiver to a transport medium (line 110). The line 110 is connected to a tip input 140 and a ring input 142 of the receiver portion of transceiver 150 via a transformer 120. A resistor 130 is used to provide an impedance for matching the impedance of line 110. For example, a T1 line according to the ANSI T1 specification has a nominal terminating impedance at the interface of 100 ohms. The T1 specification also specifies a return loss with respect to 100 ohms over the frequency band from 100 kHz to 1Mhz of at least 26 dB.

The return loss is determined by the equation:

$20 \log10 [(Z_T + Z_L)/Abs(Z_T - Z_L)]$, where Z_T is the impedance of the line interface, Z_L is the impedance of the line, and Abs is the absolute value function. It is clear that the closer Z_T is to Z_L, the higher the return loss. If Z_T is not close enough to Z_L, the return loss requirement of the T1 specification will not be met. The term "substantially match" used herein denotes meeting the specification of the transport protocol.

In this prior art line interface, if the transceiver is subsequently connected to a transport medium that has a different impedance requirement, then the external resistor is physically replaced with a corresponding resistor. For example, a J1 line requires a nominal termination impedance of 110 ohms; an E1 line (coax line) requires a nominal termination impedance of 75 ohms; and an E1 line (twisted pair line) requires a nominal termination impedance of 120 ohms. In the prior art line interface, the external resistor would be switched to match the nominal termination impedance of the new transport medium and transport protocol.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a prior art line interface for connecting a receiver to a transport medium.

FIG. 2 shows an exemplary line interface for a receiver having a programmable resistor to receive data across transport mediums having different impedance requirements.

FIG. 3 shows a block diagram of one embodiment of an exemplary adjustable resistor circuit R_Y in an IC receiver.

FIG. 4 shows a flowchart showing an example of setting the effective termination resistance RT to a predetermined value.

FIG. 5 shows one embodiment of resistor circuit block 310 that allows trimming of the resistance.

FIG. 6 shows a flowchart of the process of trimming one of the resistor circuit blocks 310 and 320 of the adjustable resistance R_Y.

DETAILED DESCRIPTION

In the following description, for the purposes of explanation, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art that the present invention may be practiced without some of these specific details. In other instances, well-known structures and devices are shown in block diagram form to avoid obscuring the underlying principles of the present invention.

AN EXEMPLARY LINE INTERFACE

Figure 2 shows an exemplary line interface for a receiver having a programmable resistor to receive data across transport mediums having different impedance requirements. For example, a transport medium such as line 210 may carry any of several different transport protocols such as those previously mentioned. In one case, line 210 may carry a transport protocol having an impedance requirement of 100 ohms. In another case, or at a different point in time, the line 210 may carry a transport protocol having an impedance requirement of 110 ohms. Alternatively, the line 210 may have an impedance requirement of 120 ohms.

A 1:1 transformer 220 and an external resistor 230 couple line 210 to a receiver portion of integrated circuit (IC) transceiver 250 at receiver tip and ring inputs 240 and 242. The IC transceiver has an adjustable resistance R_Y 260 that is electrically programmable. The combined effective resistance of both the external resistor 230 in parallel with the adjustable resistance R_Y 260 is used to match the

impedance of the line 210. Because the IC transceiver 250 has an adjustable resistance R_Y, the line interface 200 is able to match the impedances of line 210 for various transport protocols and transport mediums without the need to physically change the external resistor 230.

The use of an adjustable resistance R_Y 260 in the IC transceiver facilitates the process of switching from one transport medium to another since modification of the resistance can be done in software. Additionally, by keeping adjustable resistance R_Y 260 relatively low compared to R_X, the majority of power dissipation will be in the external resistor R_X and not in the IC.

Figure 3 shows a block diagram of one embodiment of an exemplary adjustable resistor circuit R_Y 260 in an IC receiver 250. One resistor circuit block 310 is enabled to provide a first IC resistance. Alternatively, the other resistor circuit block 320 is enabled to provide a second IC resistance. A register 330 is used to select whether either resistor circuit block 310 or 320 is enabled or disabled. This is done via transmission gates or other well-known means.

In this embodiment, an effective termination resistance R_T comprises the internal IC resistance in parallel with the external resistance R_X. Thus, the effective termination resistance of the parallel resistors is

$R_T = R_X R_Y/(R_X+R_Y)$, where R_X is the external resistance, and R_Y is the internal IC resistance.

If both resistor circuit blocks 310 and 320 are disabled, then R_Y is an open circuit and the effective termination resistance R_T is merely the external resistor R_X.

In one embodiment, the external resistor R_X has a value of 121 ohms +/- 1%, and resistor circuit blocks 310 and 320 in parallel with R_X provide an effective termination resistance R_T of 100 ohms +/- 5% and 110 ohms +/- 5%, respectively. If both resistor blocks 310 and 320 are disabled, an effective termination resistance R_T of 120 ohms +/- 5% is provided. Of course, additional resistor blocks can be added and/or the resistor blocks could provide other effective termination resistance values such as 75 ohms (e.g., for an E1 coaxial cable). However, lower resistances dissipate more power in the receiver. One alternative for the line termination to accommodate 75 ohms +/- 5% is by inserting an external balun (transformer) between the line 210 and the transformer 230. The programmable resistor R_Y and an external balun can be used in combination for providing a 75 ohms +/- 5% line termination.

Figure 4 shows a flowchart showing an example of setting the effective termination resistance R_T to a predetermined value. Typically this procedure is done upon initialization when a new line 210 is attached to the transceiver.

The flowchart starts at box 400 and proceeds to box 410 at which a write to register 330 is performed. The bit value written to register 330 determines whether to enable either resistor circuit 310 or 320 or neither circuit block based on the

desired R_T to match the new line 210. Based on the value written to register 330, the adjustable resistor R_Y's value is changed as shown in box 420.

Figure 5 shows one embodiment of resistor circuit block 310 that allows trimming of the resistance. Trimming is a way of fine tuning the resistance value of the resistor circuit because the resistance provided by resistors on an IC may vary by up to around 20% due to variations in process, temperature, and voltage. In one embodiment, seven pairs of resistors are coupled in parallel with transmission gates M15, M10, M5, 0, P5, P10, and P15 between the resistor pairs as shown in Figure 5. A trim register (not shown) is used to enable or disable particular transmission gates. For example, various combinations of 3-bit values written to the trim register can result in each of the resistor configurations shown in Table 1 (below). In this embodiment, the resistors are set up so that a nominal resistance R_{YNOM} is provided when transmission gates 0, P5, P10 and P15 are enabled, but transmission gates M5, M10 and M15 are disabled. In this embodiment, if the nominal resistance R_{YNOM} differs from the resistance value desired, then a resistor is either enabled to lower R_{YNOM} or disabled to raise R_{YNOM}.

For example, in this embodiment, the value of R_{M5} is selected such that when it is enabled (by enabling gate M5), R_{YNOM} is reduced by 5%. Similarly, R_{M10} is selected such that when it is enabled, R_{YNOM} is reduced by 10%; and R_{M15} reduces R_{YNOM} by 15% when enabled. Additionally, R_{P5} is selected such that when it is disabled, R_{YNOM} increases by 5%; R_{P10} when disabled increases R_{YNOM} by 10%; and R_{P15} when disabled increases R_{YNOM} by 15%. Table 1 shows the various

configurations of transmission gates and the corresponding resistance of the adjustable resistor circuit as was just described. An 'X' in the table indicates the transmission gate is enabled. It should be noted that there is no IC resistor configuration that uses a single path of resistance between RTIP 240 and RRING 242. This helps reduce electron migration which improves the lifetime of the IC resistors.

R_{M15}	R_{M10}	R_{M5}	R_0	R_{P5}	R_{P10}	R_{P15}	Resistance
			X	X	X	X	R_{YNOM}
			X		X	X	1.05 R_{YNOM}
			X	X		X	1.10 R_{YNOM}
			X	X	X		1.15 R_{YNOM}
		X	X	X	X	X	.95 R_{YNOM}
	X		X	X	X	X	.90 R_{YNOM}
X			X	X	X	X	.85 R_{YNOM}

Table 1.

Because the total current flowing through parallel resistors is the same as the current flowing through an equivalent resistor, the following equations

$$I = V/R_{EQ} = V/R1 + V/R2 + V/R3 + ...$$

and $R_{EQ} = 1 / (1/R1 + 1/R2 + 1/R3 + ...)$

allow us to convert the various configurations of enabled resistors shown in Table 1 into the following equations:

$$1/(\ (1/2R_0) + (1/2R_{P5}) + (1/2R_{P10}) + (1/2R_{P15})\ ) = R_{YNOM} \quad \text{(EQ. 2)}$$

$$1/(\ (1/2_{R0}) + (1/2R_{P10}) + (1/2R_{P15})\ ) = 1.05\ R_{YNOM} \quad \text{(EQ. 3)}$$

$$1/(\ (1/2R_0) + (1/2R_{P5}) + (1/2R_{P15})\ ) = 1.10\ R_{YNOM} \quad \text{(EQ. 4)}$$

$$1/(\ (1/2R_0) + (1/2R_{P5}) + (1/2R_{P10})\ ) = 1.15\ R_{YNOM} \quad \text{(EQ. 5)}$$

$$1/(\ (1/2\ R_{M5}) + (1/2R_0) + (1/2R_{P5}) + (1/2R_{P10}) + (1/2R_{P15})\ ) = .95\ R_{YNOM} \quad \text{(EQ. 6)}$$

$$1/(\ (1/2\ R_{M10}) + (1/2R_0) + (1/2R_{P5}) + (1/2R_{P10}) + (1/2R_{P15})\ ) = .90\ R_{YNOM} \quad \text{(EQ. 7)}$$

$$1/(\ (1/2\ R_{M15}) + (1/2R_0) + (1/2R_{P5}) + (1/2R_{P10}) + (1/2R_{P15})\ ) = .85\ R_{YNOM} \quad \text{(EQ. 8)}$$

If R_0 is chosen to be the smallest resistor in the resistor circuit and is used as a unit resistor, then $R_{M5} = k_{M5}*R_0$, $R_{M10} = k_{M10}*R_0$, $R_{M15} = k_{M15}*R_0$, $R_{P5} = k_{P5}*R_0$, $R_{P10} = k_{P10}*R_0$, and $R_{P15} = k_{P15}*R_0$, where k_{M5}, k_{M10}, k_{M15}, k_{P5}, k_{P10}, and k_{P15} are unit resistor coefficients. Solving for equations 2-8 for the unit resistor coefficients yields the following approximations (rounded to nearest half integer): $R_{M5} = 14*R_0$, $R_{M10} = 6.5*R_0$, $R_{M15} = 4*R_0$, $R_{P5} = 15*R_0$, $R_{P10} = 8*R_0$, $R_{P15} = 5.5*R_0$.

As an example, for an effective termination resistance of 100 ohms, and external resistor R_X of 121 ohms:

$R_{YNOM} = (R_X * R_T) / (R_X-R_T) = (121*100) / (121-100) = 576$ ohms, and

$R_0 = 396$ ohms.

For an effective termination resistance of 110 ohms, and external resistor R_X of 121 ohms:

$R_{YNOM} = (R_X * R_T) / (R_X-R_T) = (121*110) / (121-110) = 1210$ ohms, and

$R_0 = 831$ ohms.

Note that for the actual implementation of the programmable integrated circuit resistor, the unit resistor values are adjusted for the finite on-resistance of the transmission gates and for the rounding of the unit resistor coefficients. The resistor values may also be adjusted for contact and metal resistances.

Figure 6 shows a flowchart showing the process of trimming one of the circuit blocks 310 or 320. In one embodiment, both resistor circuit blocks 310 and 320 are trimmed identically since the resistance variation due to process is consistent across the IC. Thus, the same resistors would be enabled and disabled in each resistor circuit block.

The flowchart starts at block 600 and proceeds to block 610 at which the IC resistance R_Y is determined. This may be done using an IC tester or an ohm-meter. Once the value of the resistor circuit is determined, it may be modified in block 620

by enabling or disabling the appropriate resistor to decrease or increase the resistance. In one embodiment, only one resistor is enabled or disabled, and each of the resistors adds an increment or decrement of a predetermined percentage of the resistance. For example, the resistance can be increased or decreased by 5%, 10%, or 15%.

After the resistance has been trimmed to the desired value, further trimming of the resistance value R_Y may optionally be disabled (block 630). This may be done by a variety of different methods including blowing a fuse on the IC. Subsequently, a resistor circuit block could be enabled or disabled but the resistance value of the resistor circuit block could no longer be trimmed.

Thus, an apparatus and method for a programmable line interface for impedance matching is described. Throughout the foregoing description, for the purposes of explanation, numerous specific details were set forth in order to provide a thorough understanding of the invention. It will be apparent, however, to one skilled in the art that the invention may be practiced without some of these specific details. For example, the programmable resistance could be accomplished by resistors in series as well as in parallel; and the IC may have multiple independent receivers and/or transceivers, each capable of coupling to line interfaces with different effective termination resistances. Accordingly, the scope and spirit of the invention should be judged in terms of the claims that follow.

CLAIMS

WHAT IS CLAIMED IS:

1. A line interface for coupling to a first transport medium, the line interface comprising:

an integrated circuit comprising a programmable resistor; and

an external resistor coupled in parallel with the programmable resistor to provide a first effective impedance to substantially match an impedance of the first transport medium.

2. The line interface of claim 1, wherein the programmable resistor and the external resistor are coupled to provide a second effective impedance to substantially match an impedance of a second transport medium, wherein the impedance of the first transport medium is different from the impedance of the second transport medium.

3. The line interface of claim 2, wherein the impedance of the second transport medium substantially matches 75 ohms, 100 ohms or 110 ohms.

4. The line interface of claim 2, wherein the first transport medium is a T1 line and the second transport medium is a J1 line.

5. The line interface of claim 2, wherein the first transport medium is a T1 line and the second transport medium is a E1 line.

6. The line interface of claim 1, wherein the programmable resistor and external resistor are coupled to provide a second impedance to substantially match an impedance of a second transport medium responsive to a write to a register of the integrated circuit.

7. The line interface of claim 1, wherein the impedance of the first transport medium substantially matches 75 ohms, 100 ohms or 110 ohms.

8. The line interface of claim 1, wherein the programmable resistor can be disabled, and wherein the external resistor substantially matches 120 ohms.

9. The line interface of claim 1, wherein the integrated circuit comprises a second programmable resistor to couple to a secondary transport medium.

10. The line interface of claim 9, wherein the first transport medium has a first impedance and the secondary transport medium has a second impedance, and wherein the first impedance is different from the second impedance.

11. An integrated circuit comprising:

a receiver to receive a signal from a transport medium, the receiver having a ring input and a tip input; and

a programmable resistor to provide a resistance between the ring input and the tip input, the resistance being electronically programmable.

12. The integrated circuit of claim 11 further comprising:

a register coupled to the programmable resistor, wherein the resistance is electronically programmed by writing to the register.

13. The integrated circuit of claim 12, wherein the programmable resistor is comprised of a plurality of parallel resistors, and wherein a portion of the plurality of parallel resistors is enabled via a value written to the register.

14. The integrated circuit of claim 12, wherein the programmable resistor is comprised of a plurality of resistors and transmission gates coupled to the plurality of resistors, and wherein the transmission gates are controlled by writing to the register.

15. A method of tuning a resistance of an integrated circuit (IC) comprising:

determining the resistance of the IC corresponding to a first configuration of parallel resistors, wherein a portion of the parallel resistors are enabled;

modifying the resistance of the IC by creating a second configuration of parallel resistors, wherein a different portion of the parallel resistors are enabled.

16. The method of claim 15 wherein the modifying the resistance is performed by writing to a register on the IC.

17. The method of claim 15 further comprising:

permanently disabling a subsequent modification of the second configuration of parallel resistors.

18. The method of claim 17 further comprising:

controlling the entire second configuration of parallel resistors to be enabled and disabled.

19. The method of claim 17, wherein permanently disabling of a subsequent modification is achieved by blowing a fuse on the IC.

20. The method of claim 15, wherein modifying the resistance of the IC is performed by enabling a resistor of the parallel resistors to reduce the resistance of the IC by a predetermined percentage.

21. The method of claim 15, wherein modifying the resistance of the IC is performed by disabling a resistor of the parallel resistors to increase the resistance of the IC by a predetermined percentage.

22. In a line interface having a programmable resistor, a method of matching an impedance of a transport medium comprising:

writing to a register that controls the programmable resistor; and

changing the programmable resistor to provide an effective impedance substantially matching the impedance of the transport medium responsive to writing to the register.

23. The method of claim 22 wherein changing the programmable resistor is accomplished by disabling the programmable resistor.

24. The method of claim 22 further comprising:

coupling the line interface to the transport medium.

25. The method of claim 24, wherein the transport medium supports a T1, J1, or E1 transport protocol.

26. The method of claim 22 wherein the programmable resistor is changed to provide the effective impedance of 75 ohms, 100 ohms, 110 ohms, or 120 ohms.

ABSTRACT OF THE DISCLOSURE

A line interface capable of connecting to a variety of transport mediums, each having a different impedance. The line interface comprises a programmable resistor. The programmable resistor along with an external resistor provide a range of resistor values which are used to substantially match the impedance requirements of the various transport mediums.

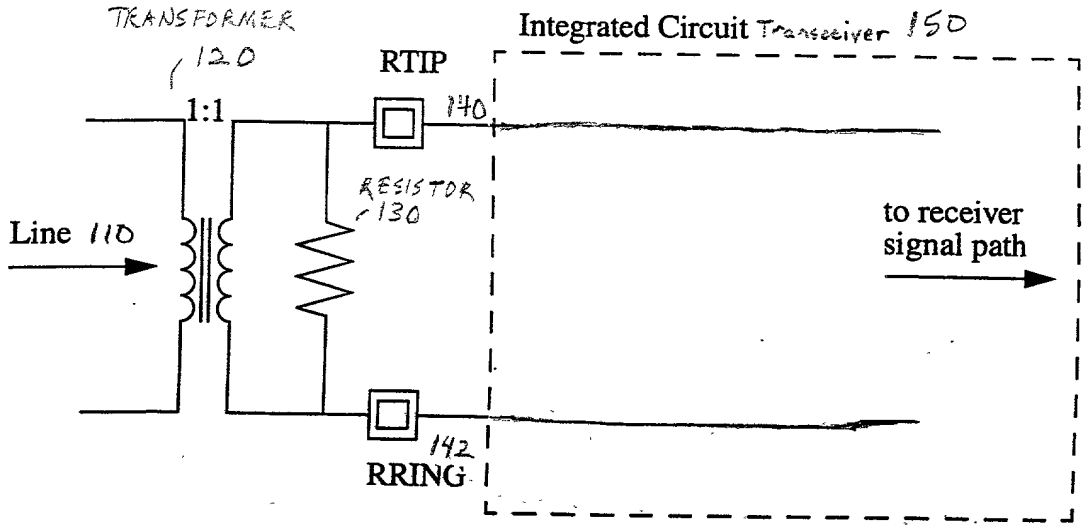


FIG. 1

(PRIOR ART)

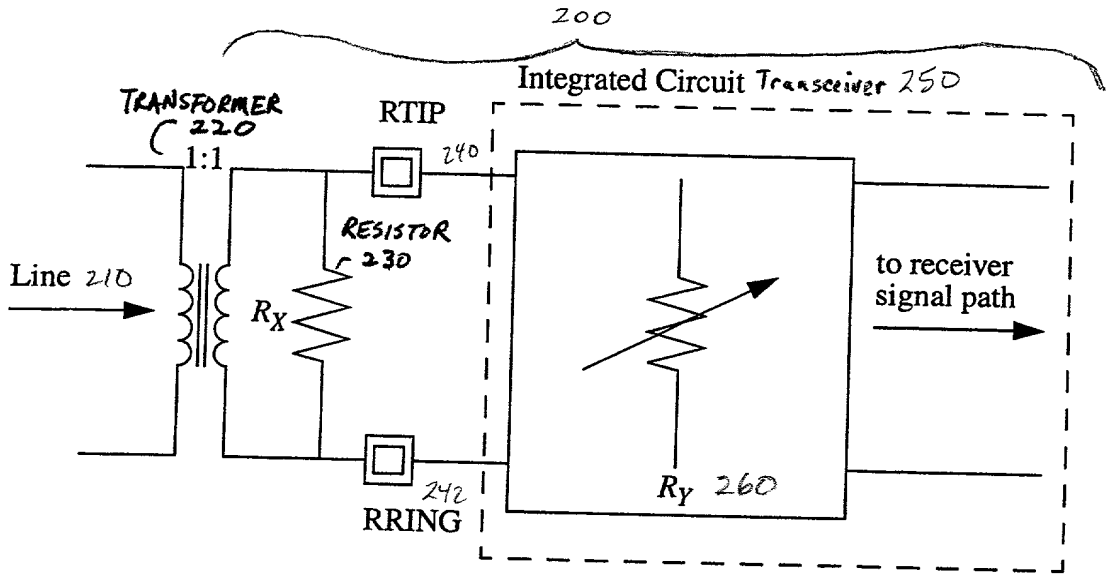


FIG. 2

FIG. 3

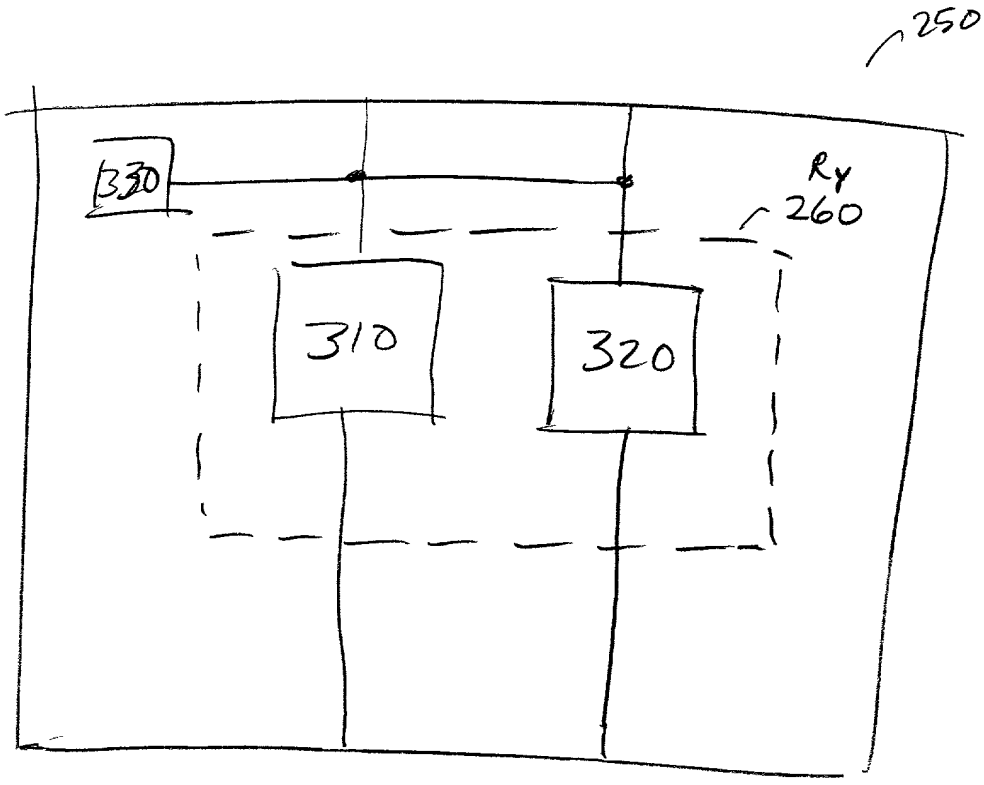
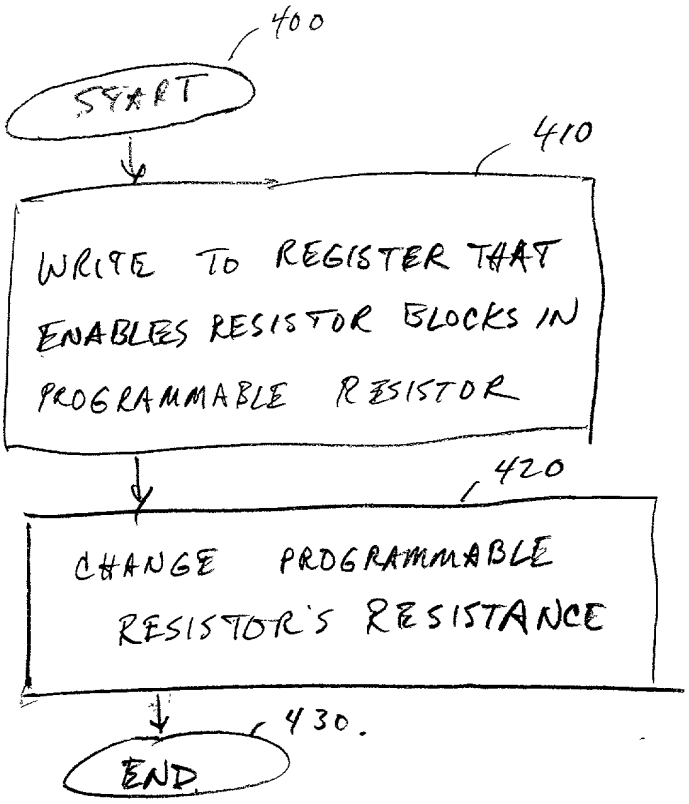


FIG 4


400
START
410
WRITE TO REGISTER THAT ENABLES RESISTOR BLOCKS IN PROGRAMMABLE RESISTOR
420
CHANGE PROGRAMMABLE RESISTOR'S RESISTANCE
430.
END

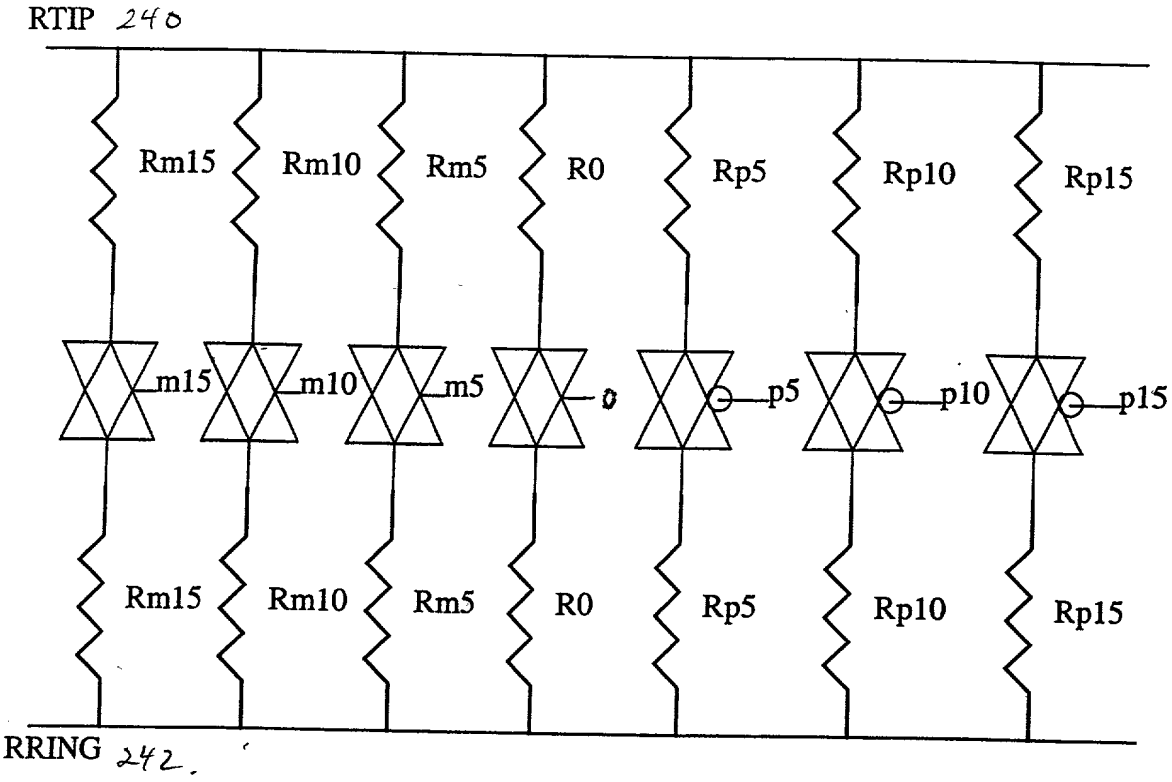
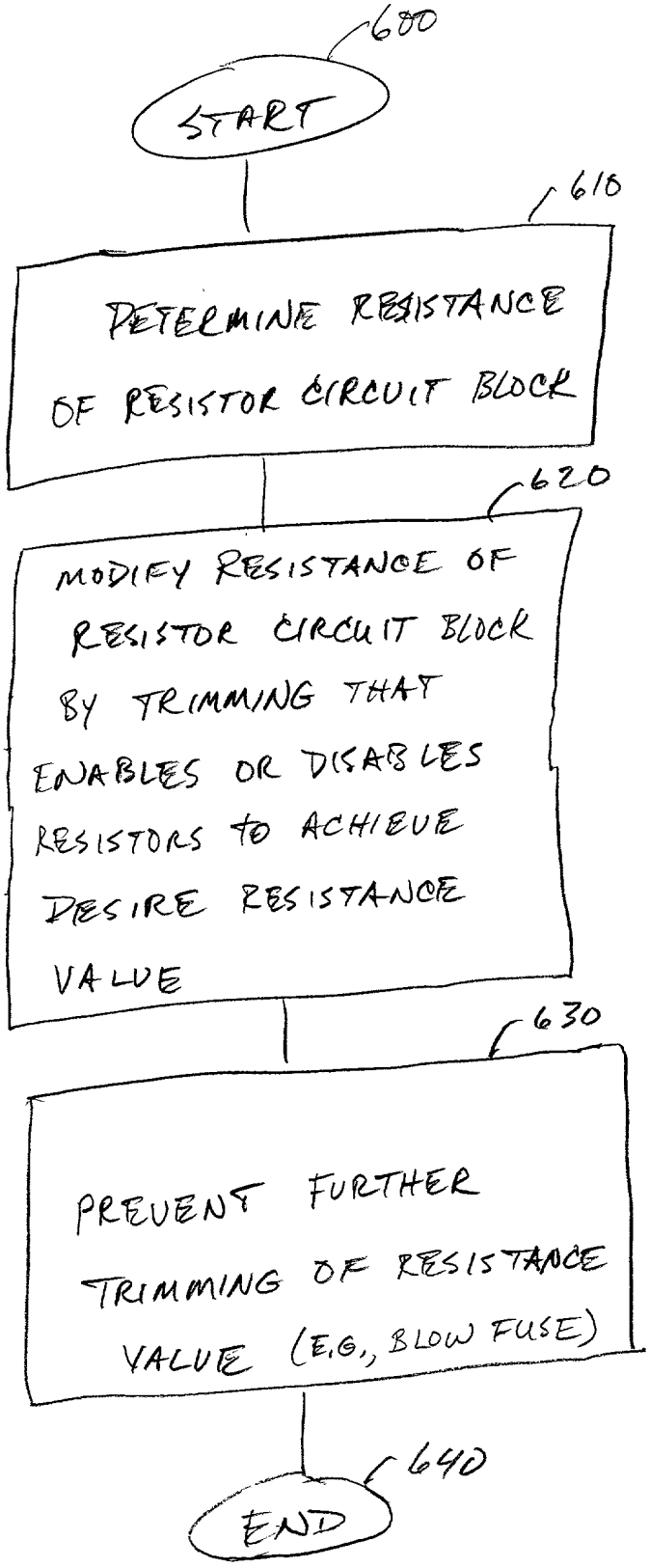

RTIP 240
Rm15
Rm10
Rm5
R0
Rp5
Rp10
Rp15
m15
m10
m5
0
p5
p10
p15
Rm15
Rm10
Rm5
R0
Rp5
Rp10
Rp15
RRING 242

Figure 5

FIG. 6


600
START
610
DETERMINE RESISTANCE OF RESISTOR CIRCUIT BLOCK
620
MODIFY RESISTANCE OF RESISTOR CIRCUIT BLOCK BY TRIMMING THAT ENABLES OR DISABLES RESISTORS TO ACHIEVE DESIRE RESISTANCE VALUE
630
PREVENT FURTHER TRIMMING OF RESISTANCE VALUE (E.G., BLOW FUSE)
640
END

Attorney's Docket No.: 42390.P8718 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
Apparatus and Method for Programmable Line Interface Impedance Matching

the specification of which

XXX is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number_____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned
Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Charles K. Young, BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to Charles K. Young, (408) 720-8300.
(Name of Attorney or Agent)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's Signature Russell Byrd Date 08/28/00

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Inventor's Signature _____ Date _____

Residence _____ (City, State) Citizenship _____ (Country)

Post Office Address _____

APPENDIX A

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APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.